

Dual 1A, 1.25MHz Synchronous Step-Down Converter

General Description

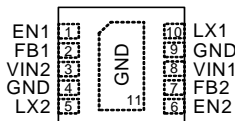
The RT8075 is a high efficiency Pulse-Width-Modulated (PWM) dual step-down DC/DC converter. Capable of delivering up to 1A output current over a wide input voltage range from 2.5V to 5.5V, the RT8075 is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources such as cellular phones, PDAs, PC WLAN card and hand-held devices.

Three operating modes are available including : PWM mode, Low Dropout Mode and shut-down mode. The Internal synchronous rectifier with low $R_{DS(ON)}$ dramatically reduces conduction loss at PWM mode. No external Schottky diode is required in practical application. The RT8075 enters Low Dropout mode when normal PWM cannot provide regulated output voltage by continuously turning on the upper P-MOSFET. The RT8075 enters shut-down mode and consumes less than 0.1 μ A when the EN pin is pulled low.

The switching ripple is easily smoothed-out by small package filtering elements due to the fixed operating frequency of 1.25MHz. The RT8075 is available in the WDFN-10L 3x3 package.

Pin Configurations

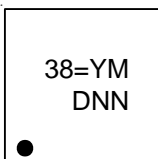
(TOP VIEW)



WDFN-10L 3x3

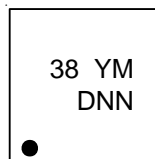
Marking Information

RT8075GQW



38= : Product Code
YMDNN : Date Code

RT8075ZQW



38 : Product Code
YMDNN : Date Code

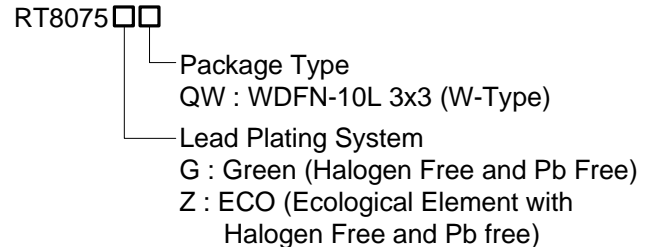
Features

- 2.5V to 5.5V Input Range
- 1A Output Current
- 1.25MHz Fixed Frequency PWM Operation
- 95% Efficiency
- No Schottky Diode Required
- 0.6V Reference Allows Low Output Voltage
- Low Dropout Operation : 100% Duty Cycle
- Small 10-Lead WDFN Package
- RoHS Compliant and Halogen Free

Applications

- Portable Instruments
- Microprocessors and DSP Core Supplies
- Cellular Phones
- Wireless and DSL Modems
- PC Cards

Ordering Information

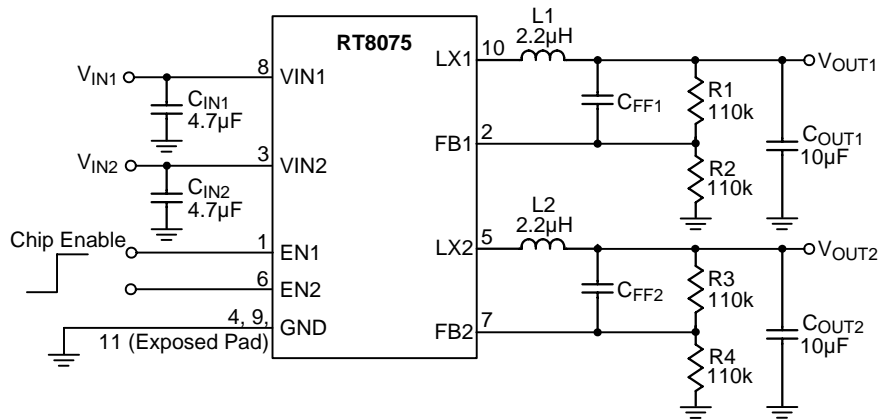


Note :

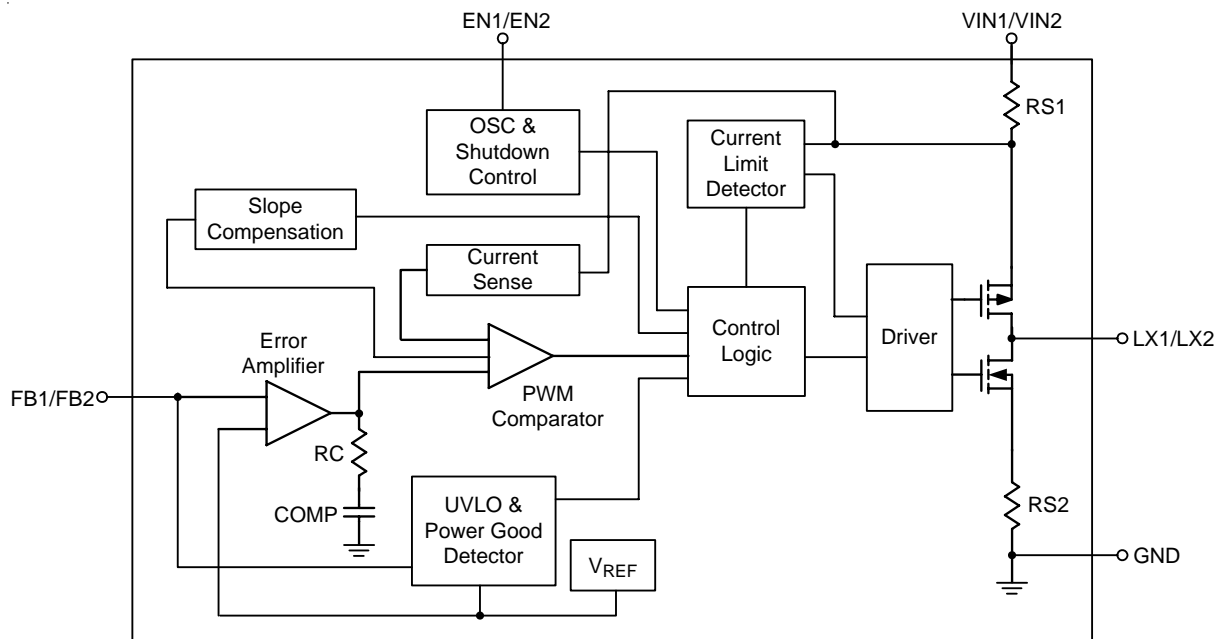
Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Typical Application Circuit



Function Block Diagram



Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|------------------------|----------|---|
| 1 | EN1 | Chip Enable of Channel 1 (Active High). |
| 2 | FB1 | Feedback Input of Channel 1. |
| 3 | VIN2 | Power Supply Input of Channel 2. |
| 5 | LX2 | Switching Node of Channel 2. |
| 6 | EN2 | Chip Enable of Channel 2 (Active High). |
| 7 | FB2 | Feedback Input of Channel 2. |
| 8 | VIN1 | Power Supply Input of Channel 1. |
| 10 | LX1 | Switching Node of Channel 1. |
| 4, 9, 11 (Exposed Pad) | GND | Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. |

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage V_{IN1}, V_{IN2} ----- -0.3V to 6.5V
- LX1, LX2 Pin Voltage ----- -0.3V to ($V_{IN} + 0.3V$)
- Other Pins Voltage ----- -0.3V to 6.5V
- Power Dissipation, P_D @ $T_A = 25^\circ C$
 WDFN-10L 3x3 ----- 1.471W
- Package Thermal Resistance (Note 2)
 WDFN-10L 3x3, θ_{JA} ----- 68°C/W
 WDFN-10L 3x3, θ_{JC} ----- 7.8°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
 HBM (Human Body Mode) ----- 2kV
 MM (Machine Mode) ----- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ----- 2.5V to 5.5V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

Electrical Characteristics

($V_{IN} = 3.6V, T_A = 25^\circ C$ unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------------|----------------|---|-------|------|----------|----------|
| Input Voltage Range | V_{IN} | | 2.5 | -- | 5.5 | V |
| Reference Voltage | V_{REF} | | 0.588 | 0.6 | 0.612 | V |
| Quiescent Current | I_Q | $I_{OUT} = 0mA, V_{FB} = V_{REF} + 5\%$ | -- | 70 | -- | μA |
| Shutdown Current | I_{SHDN} | | -- | 0.1 | 1 | μA |
| Under Voltage Lockout Threshold | UVLO | V_{IN} Rising | -- | 2.1 | -- | V |
| | | Hysteresis | -- | 0.18 | -- | |
| Oscillator Frequency | f_{OSC} | $V_{IN} = 3.6V, I_{OUT} = 300mA$ | 1 | 1.25 | 1.5 | MHz |
| EN1 High-Level Input Voltage | V_{EN_H} | $V_{IN} = 2.5V$ to 5.5V | 1.5 | -- | V_{IN} | V |
| EN1 Low-Level Input Voltage | V_{EN_L} | $V_{IN} = 2.5V$ to 5.5V | -- | -- | 0.4 | |
| Thermal Shutdown Temperature | T_{SD} | | -- | 160 | -- | °C |
| Peak Current Limit | I_{LIM} | $V_{IN} = 2.5V$ to 5.5 V | 1.2 | 1.5 | 2.1 | A |
| Switch On Resistance, High | $R_{DS(ON)_P}$ | $I_{OUT} = 200mA, V_{IN} = 3.6V$ | -- | 0.25 | -- | Ω |
| Switch On Resistance, Low | $R_{DS(ON)_N}$ | $I_{OUT} = 200mA, V_{IN} = 3.6V$ | -- | 0.26 | -- | Ω |
| Output Line Regulation | | $V_{IN} = 2.5V$ to 5.5V (Note 5) | -- | 0.04 | 0.4 | %/V |
| Output Load Regulation | | $50mA < I_{LOAD} < 1A$ (Note 5) | -- | 0.5 | -- | % |

Note 1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at $T_A = 25^\circ\text{C}$ on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the exposed pad of the package.

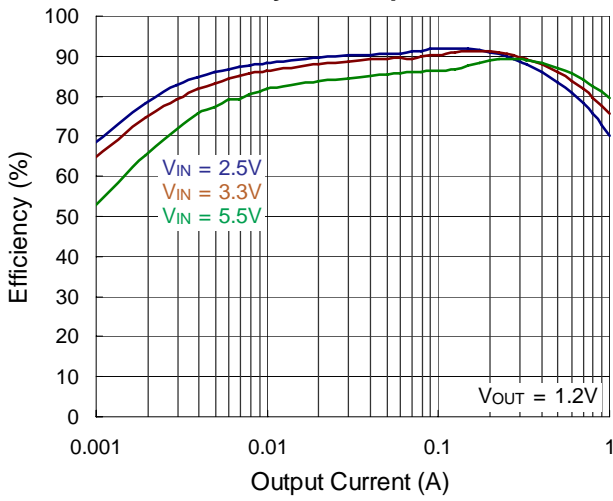
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

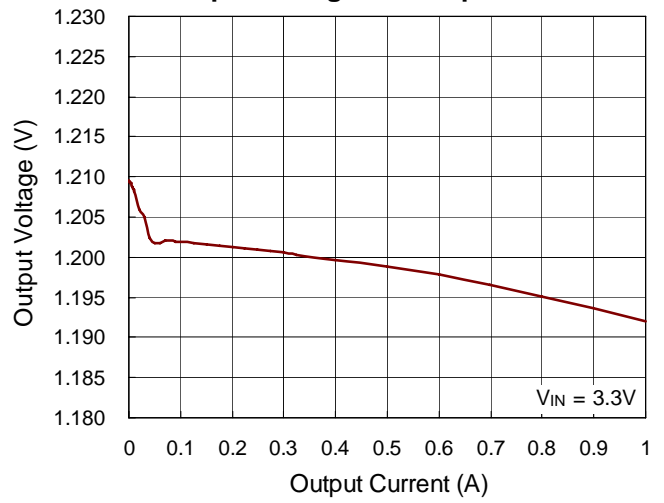
Note 5. Guarantee by design.

Typical Operating Characteristics

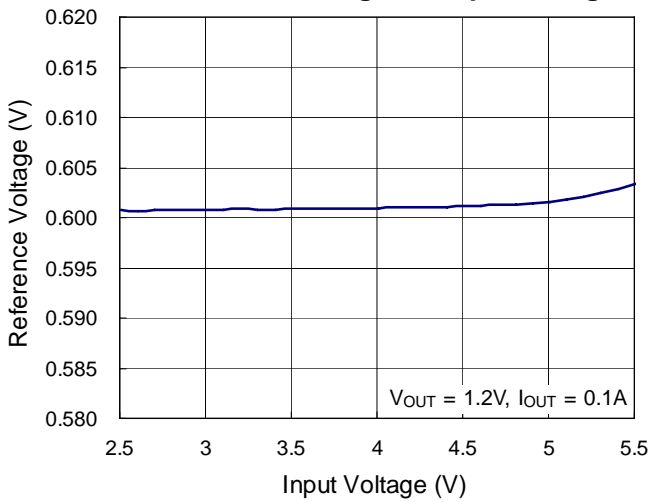
Efficiency vs. Output Current



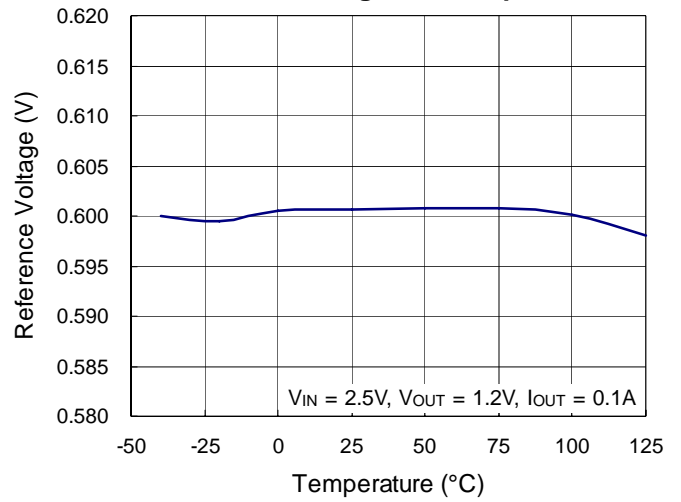
Output Voltage vs. Output Current



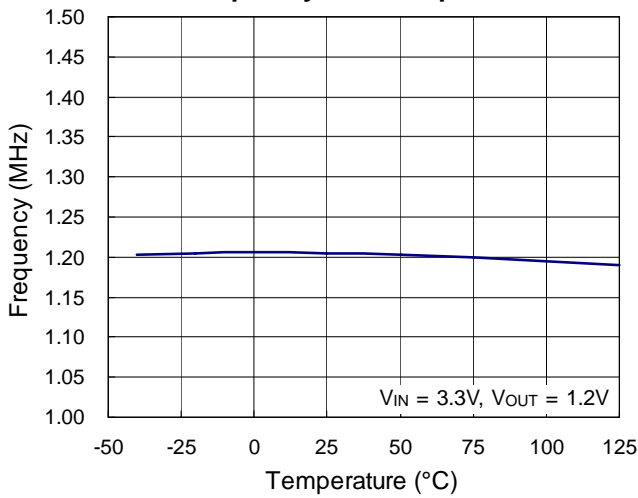
Reference Voltage vs. Input Voltage



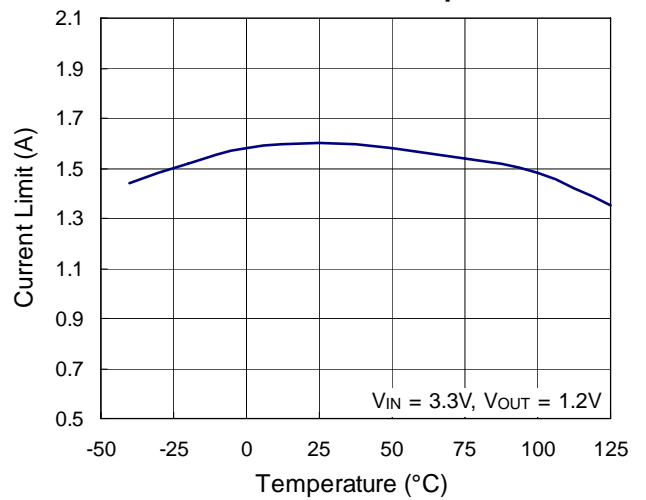
Reference Voltage vs. Temperature



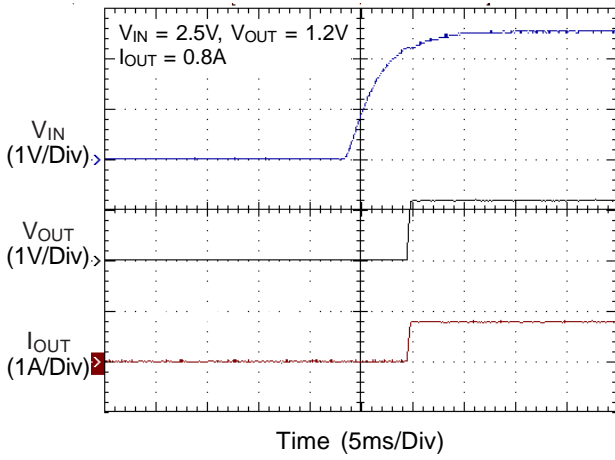
Frequency vs. Temperature



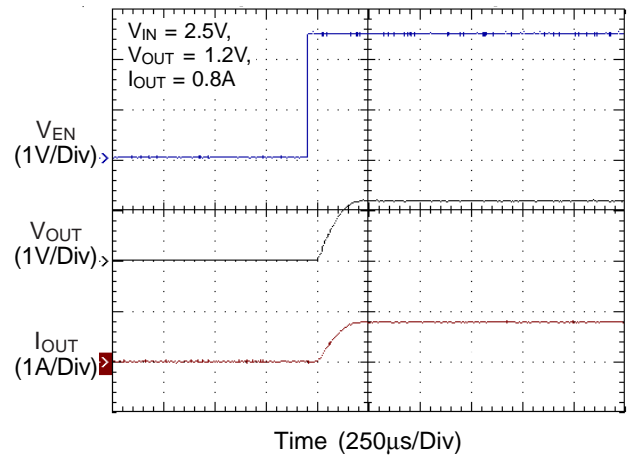
Current Limit vs. Temperature



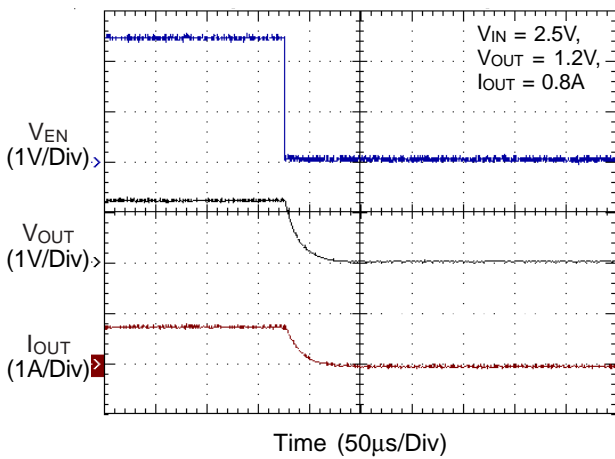
Power On from V_{IN}



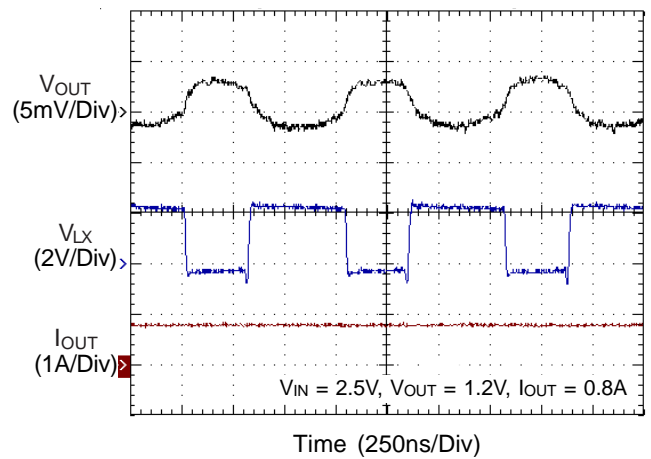
Power On from EN



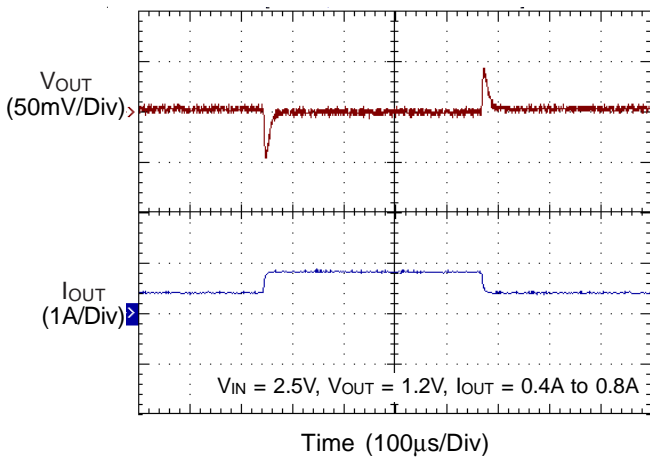
Power Off from EN



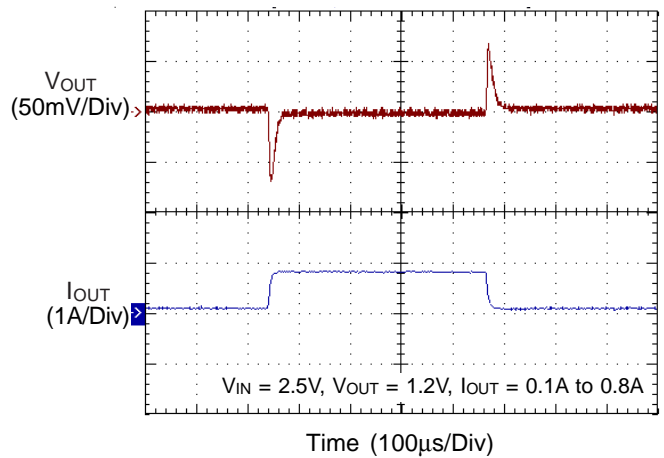
Switching



Load Transient Response



Load Transient Response



Applications Information

The basic RT8075 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L} \right] \times \left[1 - \frac{V_{OUT}}{V_{IN}} \right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is ΔI_L = 0.4(I_{MAX}). The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}} \right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right]$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or mollypermalloy cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard”, which means that inductance collapses abruptly when the peak design

current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor.

Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs size requirements and any radiated field/EMI requirements.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V_{IN} = 2V_{OUT}, where I_{RMS} = I_{OUT}/2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the Effective Series Resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN} . At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Output Voltage Setting

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

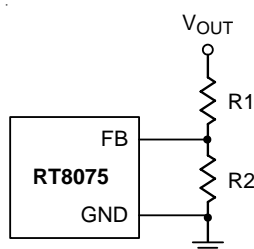


Figure 1. Setting Output Voltage

For adjustable voltage mode, the output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF} \left(1 + \frac{R1}{R2} \right)$$

where V_{REF} is the internal reference voltage (0.6V typ.)

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} (ESR)$, where ESR is the effective series resistance of C_{OUT} . ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of the RT8075, The maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WDFN-10L 3x3 package, the thermal resistance θ_{JA} is 68°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (68^\circ\text{C/W}) = 1.471\text{W for WDFN-10L 3x3}$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA} . For RT8075 package, the Figure 2 of derating curve allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

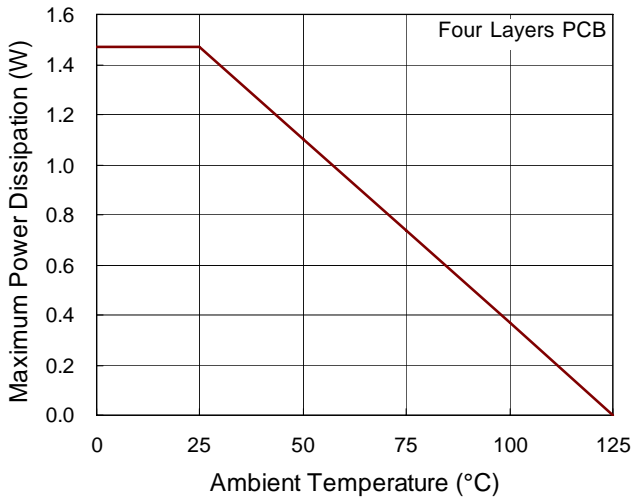


Figure 2. Derating Curves for RT8075 Package

Layout Considerations

Follow the PCB layout guidelines for optimal performance of RT8075.

- ▶ Keep the trace of the main current paths as short and wide as possible.
- ▶ Put the input capacitor as close as possible to the device pins (VIN1 / VIN2 and GND).
- ▶ LX 1 / LX 2 node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the LX 1 / LX 2 node to prevent stray capacitive noise pick-up.
- ▶ Place the feedback components as close as possible to the FB1 / FB2 pins.
- ▶ The GND and Exposed Pad must be connected to a strong ground plane for heat sinking and noise protection.

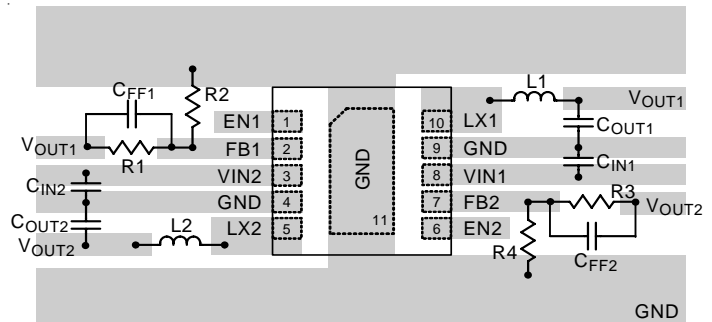


Figure 3. PCB Layout Guide

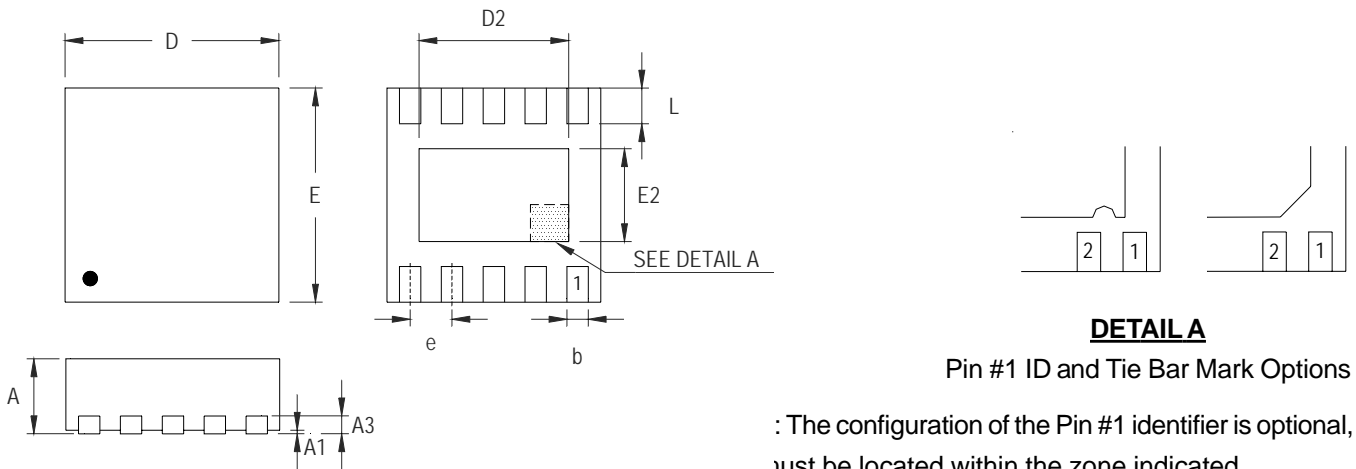
Table 1. Recommended Inductors

| Supplier | Inductance (mH) | Dimensions (mm) | Series |
|-------------|-----------------|--------------------|----------|
| TAIYO YUDEN | 2.2 | 3.00 x 3.00 x 1.50 | NR 3015 |
| GOTREND | 2.2 | 3.85 x 3.85 x 1.80 | GTSD32 |
| Sumida | 2.2 | 4.50 x 3.20 x 1.55 | CDRH2D14 |
| Sumida | 4.7 | 4.50 x 3.20 x 1.55 | CDRH2D14 |
| TAIYO YUDEN | 4.7 | 3.00 x 3.00 x 1.50 | NR 3015 |
| GOTREND | 4.7 | 3.85 x 3.85 x 1.80 | GTSD32 |

Table 2. Recommended Capacitors for C_{IN} and C_{OUT}

| Supplier | Capacitance (mF) | Package | Part Number |
|-------------|------------------|---------|-------------------|
| TDK | 4.7 | 0603 | C1608JB0J475M |
| MURATA | 4.7 | 0603 | GRM188R60J475KE19 |
| TAIYO YUDEN | 4.7 | 0603 | JMK107BJ475RA |
| TAIYO YUDEN | 10 | 0603 | JMK107BJ106MA |
| TDK | 10 | 0805 | C2012JB0J106M |
| MURATA | 10 | 0805 | GRM219R60J106ME19 |
| MURATA | 10 | 0805 | GRM219R60J106KE19 |
| TAIYO YUDEN | 10 | 0805 | JMK212BJ106RD |

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

: The configuration of the Pin #1 identifier is optional, must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.180 | 0.300 | 0.007 | 0.012 |
| D | 2.950 | 3.050 | 0.116 | 0.120 |
| D2 | 2.300 | 2.650 | 0.091 | 0.104 |
| E | 2.950 | 3.050 | 0.116 | 0.120 |
| E2 | 1.500 | 1.750 | 0.059 | 0.069 |
| e | 0.500 | | 0.020 | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |

W-Type 10L DFN 3x3 Package

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